REMARKS

Claims 1-6 and 9-17 are pending in the application. In the Final Office Action of May 5, 2004, the Examiner made the following disposition:

A.) Rejected claims 1-6 and 9-17 under 35 U.S.C. §112, first paragraph.

B.) Rejected claims 1, 3-6, and 11-13 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Yamazaki.*

C.) Rejected claim 2 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Yamazaki* and further in view of *Gowda.*

D.) Rejected claims 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Yamazaki* and further in view of *Munier.*

E.) Rejected claims 14-17 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Yamazaki* and further in view of *Koch.*

Applicants respectfully traverse the rejections and address the Examiner's disposition as follows:

A.) Rejection of claims 1-6 and 9-17 under 35 U.S.C. §112, first paragraph:

Independent claims 1, 14 and 16 have been amended as per the Examiner's request to overcome the rejection.

Claims 2-6, 9-13, 15 and 17 depend directly or indirectly from claims 1, 14 or 16 and are therefore allowable for at least the same reasons that claims 1, 14 and 16 are allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

B.) Rejection of claims 1, 3-6, and 11-13 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Yamazaki*:

Applicants respectfully disagree with the rejection.

Claims 1, 14 and 16 have each been amended as described above in Section A. Claims 15 and 17 have each been amended to correct informalities. Claims 9 and 10 have been canceled.

Referring to Applicants' Figure 2 for illustrative purposes, Applicants' independent claims 1, 14 and 16, each as amended, each claim a selection switch 13 and a read-out switch 14 that each comprises a MOS transistor having a double gate structure, wherein each gate electrode of the selection switch 13 and the read-out switch 14 comprises a two-layer gate electrode, and neighboring portions that are overlapped with each other. The gate electrode of one of the selection switch 13 and the read-out switch 14 is connected to one of a plurality of vertical

selection lines 16 and the gate electrode of the other of the selection switch 13 and the read-out switch 14 is connected to one of a plurality of read-out pulse lines 17.

Referring to Applicants' Figure 7 for illustrative purposes, as claimed, neighboring portions of the gate electrodes 13a, 14a of the selection switch 13 and the read-out switch 14 are overlapped with each other, whereby the n+ diffusion region does not occur between the gate electrodes 13a, 14a. Accordingly, a noise component due to the dispersion of the field occurring in the gate electrode 14a of the read-out switch 14 at the shift timing from the period d to the period e is completely transferred. Therefore, any noise due to the gate electrode 14a of the read-out switch 14 does not occur.

Further, the overflow charge from the photodiode 12 is directly supplied to the n+ diffusion region connected to the vertical signal line 15, so that smear can be suppressed to only the charges occurring within the one pixel read-out time by resetting the vertical signal line 15 just before the signal charge (pixel signal) is read out. (*See*, page 12, paragraph 3 - page 14, paragraph 1).

This is clearly unlike *Sauer* in view of *Yamazaki*, which fails to disclose or suggest Applicants' claimed switches having a double gate structure with two-layer gate electrodes, wherein a gate electrode of one of a selection switch and a read-out switch connected to a vertical selection line and a gate electrode of the other of the selection switch and the read-out switch connected to a read-out pulse line. As stated by the Examiner, *Sauer* fails to disclose a double-gated transistor. Therefore, the Examiner combines *Sauer* with *Yamazaki* in an attempt to disclose or suggest claims 1, 14 and 16, however, Applicants respectfully submit that *Sauer* in view of *Yamazaki* still fails to disclose or suggest claims 1, 14 and 16, as amended.

Although *Yamazaki* discloses a double-gated transistor, *Sauer* in view of *Yamazaki* still fails to disclose or suggest overlapping electrodes, wherein a gate electrode of one of a selection switch and a read-out switch connected to a vertical signal line and a gate electrode of the other of the selection switch and the read-out switch connected to a horizontal signal lines. Referring to *Yamazaki* Figure 4C, *Yamazaki* discloses gate electrodes 103 and 113 that are clearly connected to horizontal signal lines 102 and 112. Unlike Applicants' independent claims 1, 14 and 16, nowhere does *Yamazaki* disclose or even suggest connecting one of its gate electrodes 103 or 112 to a vertical signal line. Applicants respectfully submit that *Yamazaki* specifically teaches away from connecting one of its gate electrodes to a vertical signal line and the other gate electrode to a horizontal signal line, because *Yamazaki* teaches that it connects both gate electrodes to horizontal transfer lines "to prevent a row in the matrix from failing even if either

the upper or lower gate line for the row is broken." (Col. 8, lines 43-45). Thus, one having skill in the art would not have looked to the combination of *Sauer* with *Yamazaki* to suggest a gate electrode of one of a selection switch and a read-out switch connected to a vertical signal line and a gate electrode of the other of the selection switch and the read-out switch connected to a horizontal signal lines. For at least this reason, *Sauer* in view of *Yamazaki* fails to disclose or suggest claims 1, 14 or 16.

Further, *Yamazaki's* two gate electrodes 103 and 113 are applied to a single element (TFT), which originally required just one electrode. Thus, *Yamazaki's* two gate electrodes 103 and 113 serve the same purpose. As described in *Yamazaki*, the two gate electrodes 103 and 113 are provided to lower the resistance compared to using a single gate electrode. Therefore, *Yamazaki* is unlike Applicants' claims 1, 14 and 16, which each claim a double gate structure (*i.e.*, a two-layer gate structure) that is applied to a set of two different elements, each having a gate electrode. Applicants' electrodes have different roles: one for a vertical selection line and the other for a read-out pulse line. Thus, *Sauer* in view of *Yamazaki* still fails to disclose or suggest Applicants' claimed a double gate structure with two-layer gate electrodes, wherein a gate electrode of one of a selection switch and a read-out switch connected to a vertical signal line and a gate electrode of the other of the selection switch and the read-out switch connected to a horizontal signal lines.

Claims 3-6, 11-13, 15 and 17 depend directly or indirectly from claims 1, 14 or 16 and are therefore allowable for at least the same reasons that claims 1, 14 and 16 are allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

C.) Rejection of claim 2 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Yamazaki* and further in view of *Gowda*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 is allowable over *Sauer* in view of *Yamazaki* as described above. *Gowda* still fails to disclose or suggest a double gate structure with two-layer gate electrodes, wherein a gate electrode of one of a selection switch and a read-out switch connected to a vertical signal line and a gate electrode of the other of the selection switch and the read-out switch connected to a horizontal signal lines. Therefore, *Sauer* in view of *Yamazaki* and further in view of *Gowda* still fails to disclose or suggest claim 1.

Claim 2 depends directly or indirectly from claim 1 and is therefore allowable for at least

the same reasons that claim 1 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

D.) Rejection of claims 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Yamazaki* and further in view of *Munier*:

Claims 9 and 10 have been canceled.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

E.) Rejection of claims 14-17 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Yamazaki* and further in view of *Koch*:

Applicants respectfully disagree with the rejection.

Applicants' independent claims 14 and 16 are allowable over *Sauer* in view of *Yamazaki* as described above. *Koch* still fails to disclose or suggest a double gate structure with two-layer gate electrodes, wherein a gate electrode of one of a selection switch and a read-out switch connected to a vertical signal line and a gate electrode of the other of the selection switch and the read-out switch connected to a horizontal signal lines. Therefore, *Sauer* in view of *Yamazaki* and further in view of *Koch* still fails to disclose or suggest claims 14 and 16.

Claims 15 and 17 depend directly or indirectly from claims 14 and 16 and are therefore allowable for at least the same reasons that claims 14 and 16 are allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-6 and 11-17 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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